REMARKS

In the Office Action, the Examiner objected to claims 34-35, 50-52 and 54 for various informalities. The Examiner rejected claims 28, 30-52, and 54 under 35 U.S.C. §102(b) as being anticipated by United States Patent 5,699,625 to Scepanovic, et al. (Scepanovic). In this Amendment, Applicants have amended claims 28, 31, 34-36, 41, 50-52 and 54, and canceled claims 30 and 40. Applicants have not added any claim. Accordingly, claims 28, 31-39, 41-52 and 54 will be pending in the application after entry of this Amendment.

I. Objection to Claims 34-35, 50-52 and 54

In the Office Action, the Examiner objected to claims 34-35, 50-52 and 54 for various informalities. Applicants have amended the claims to address the cited informalities. Accordingly, Applicants respectfully request withdrawal of the objection to these claims.

II. Rejection of Claims 28, 31-35 under §102(b)

The Examiner rejected claims 28 and 31-35 under §102(b) as being anticipated by Scepanovic. Claims 31-35 are dependent on claim 28. For a placer that places circuit modules in integrated-circuit (IC) layouts, claim 28 recites a method of pre-computing costs of placing circuit modules in an IC layout region. The placer uses a set of partitioning lines that define a plurality of slots. The slots are used to partition an IC layout region into a plurality of sub-regions corresponding to the slots. The method selects a first group of the slots. The method computes a first attribute of a set of one or more interconnect lines necessary for connecting the first group of the slots. Computing the first attribute includes calculating the length of the set of interconnect lines. The method computes a second attribute of the set of interconnect lines. The second attribute includes the number of bends in the set of interconnect lines. The method stores the

computed attributes in a storage structure for later use by the placer during a placement operation.

Applicants respectfully submit that Scepanovic does not disclose, teach, or even suggest such a method. The Examiner cites column 3, lines 10-23, and column 5, lines 7-22, of Scepanovic. The cited portion of Scepanovic describes "specifying a set of cells, a set of wiring nets for interconnecting the cells, and a set of regions on the chip in which the cells are to be placed." Scepanovic states that penalties are computed for assigning the cells to the regions such that the total penalty thereof is minimized. Scepanovic further states at column 6, line 18, that the cost or penalty is the total wirelength of the placement. However, Scepanovic does not disclose, teach, or even suggest a method that computes and stores the length of the set of interconnect lines and the number of bends in the set of interconnect lines necessary for connecting the first group of slots.

Moreover, Applicants have amended claim 28 to recite that the precomputed attributes are stored in a storage structure for later use by the placer during a placement operation. Applicants respectfully submit that Scepanovic does not disclose, teach, or even suggest any such precomputing and storing. Thus, Scepanovic does not disclose, teach, or even suggest several limitations of claim 28, as recited above.

Accordingly, Applicants respectfully submit that Scepanovic neither anticipates claim 28, nor otherwise invalidates, this claim. Since claims 31-35 are dependent on claim 28, Applicants respectfully submit that Scepanovic neither anticipates, nor otherwise invalidates, claims 31-35 for at least the reasons discussed above in relation to claim 28. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claims 28 and 31-35.

III. Rejection of Claims 36-39 and 41-49 under §102(b)

The Examiner rejected claims 36-39 and 41-49 under §102(b) as being anticipated by Scepanovic. Claims 37-39 and 41-49 are dependent on claim 36. Claim 36 recites for an electronic design automation (EDA) application that performs placement operations, a method that pre-computes costs of placing circuit elements within an integrated-circuit (IC) layout. The method defines a partitioning grid having a plurality of slots. The partitioning grid is for partitioning a region of an IC layout during a placement operation. For each combination of the slots, the method defines at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of the slots. The method computes multiple attributes for each of the connection graphs. One of the attributes includes the number of bends in several of the connection graphs. The method stores the computed attributes in a storage structure for later use by the EDA application during the placement operation.

Applicants respectfully submit that Scepanovic does not disclose, teach, or even suggest such a method. The Examiner cites column 3, lines 20-23, column 6, lines 16-32, column 8, lines 3-9, Figure 2 and column 4, lines 60-67 of Scepanovic. These portions of Scepanovic describe "specifying a hypergraph H consisting of" sets of vertices, hyperedges, and sizes of the vertices. However, the cited portions of Scepanovic do not disclose, teach, or even suggest a method that, for each combination of slots, identifies at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of the slots and computes the length and number of bends in each of the connection graphs. Moreover, since the cited portions of Scepanovic do not disclose, teach, or even suggest computing the number of bends in each connection graph, the cited portions cannot disclose storing these computed attributes (e.g., the

number of bends) in a storage structure. Thus, Scepanovic does not disclose, teach, or suggest claim 36, as recited above.

Accordingly, Applicants respectfully submit that Scepanovic neither anticipates claim 36, nor otherwise invalidates this claim. Since claims 37-39 and 41-49 are dependent on claim 36, Applicants respectfully submit that Scepanovic neither anticipates, nor otherwise invalidates, claims 37-39 and 41-49 for at least the reasons discussed above in relation to claim 36. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claims 36-39 and 41-49.

III. Rejection of Claims 50-51 under §102(b)

The Examiner rejected claims 50-52 and 54 under §102(b) as being anticipated by Scepanovic. Claim 51 is dependent on claim 50. Claim 50 recites for an electronic design automation (EDA) application that performs placement operations, a method that pre-computes costs of placing circuit elements within an integrated-circuit (IC) layout. The method defines a partitioning grid having a plurality of slots. The partitioning grid is for partitioning during a placement operation, a region of an IC layout into a plurality of sub-regions corresponding to the slots. For each combination of the slots, the method identifies at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of the slots. The method computes the length and number of bends in each of the connection graphs. The method stores the length of a connection graph identified for each combination of the slots. When more than one connection graph is defined for a combination of the slots, the method stores the length of a short connection graph that has less than a first predetermined number of bends for later use by the EDA application during the placement operation.

Applicants respectfully submit that Scepanovic does not disclose, teach, or even suggest such a method. The Examiner cites column 6, lines 16-50, to support the §102(b) rejection. This portion of Scepanovic describes "specifying a hypergraph H consisting of" sets of vertices, hyperedges, and sizes of the vertices. However, the cited portion of Scepanovic does not disclose, teach, or even suggest a method that, for each combination of slots, identifies at least one connection graph that models the topology of interconnect lines necessary for connecting the combination of the slots and computes the length and number of bends in each of the connection graphs. Moreover, since this portion of Scepanovic does not disclose, teach, or even suggest computing the number of bends in each connection graph, the cited portion cannot disclose storing the length of a short connection graph that has less than a first predetermined number of bends for later use by the EDA application during a placement operation. Thus, Scepanovic does not disclose, teach, or suggest several limitations of claim 50, as recited above.

Accordingly, Applicant respectfully submit that Scepanovic neither anticipates claim 50, nor otherwise renders this claim invalid. As claim 51 is dependent on claim 50, Applicants respectfully submit that Scepanovic neither anticipates, nor otherwise invalidates, claim 51 for at least the reasons discussed above in relation to claim 50. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claims 50-51.

IV. Rejection of Claim 52 under §102(b)

Claim 52 recites a method that places circuit modules in a region of an integrated circuit (IC) layout. The IC layout has several circuit elements. Several nets represent interconnections between the circuit elements and each net is defined to include a set of circuit elements. The method partitions the IC region into several sub-regions and selects a net. The method identifies the set of sub-regions containing the circuit elements of the selected net. The method retrieves

from a storage structure multiple pre-computed attributes of a set of one or more interconnect lines necessary for connecting the identified set of sub-regions. The method computes a placement cost of the net within the region by using the retrieved attributes. The method changes the position of a circuit element of the net from one sub-region to another. The method identifies a new set of sub-regions that contain the circuit elements of the net. The method retrieves multiple pre-computed attributes of a different set of interconnect lines necessary for connecting the identified new set of sub-regions. The method computes a new placement cost of the net within the region by using the attributes retrieved for the different set of interconnect lines. The retrieved attributes include the number of bends in the different set of interconnect lines.

Applicants respectfully submit that Scepanovic does not, disclose, teach or even suggest such a method. For instance Scepanovic does not disclose, teach, or even suggest retrieving from a storage structure multiple pre-computed attributes of a set of one or more interconnect lines necessary for connecting the identified set of sub-regions. Moreover, Applicants have amended claim 52 to recite the limitation that the retrieved attributes include the number of bends in the interconnect lines. As discussed above, Scepanovic does not disclose, teach, or even suggest this limitation. Accordingly, Applicants respectfully submit that Scepanovic neither anticipates, nor otherwise invalidates claim 52. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claim 52.

V. Rejection of Claim 54 under §102(b)

Claim 54 recites a method of placing circuit modules in a region of an integrated circuit (IC) layout. The IC layout has several circuit elements. Several nets represent interconnections between the circuit elements and each net is defined to include a set of circuit elements. The method partitions the IC-layout region into several sub-regions. For each particular net, the

method identifies the set of sub-regions containing the circuit elements of the particular net. For each particular net, the method retrieves multiple pre-computed attributes of a connection graph that models the topology of interconnect lines needed to connect the identified set of sub-regions of the particular net. The connection graph is either a Steiner tree or a minimum spanning tree. The method computes a placement cost for the IC layout within the region by using the retrieved attributes. The retrieved attributes include the number of bends in each of the connection graphs.

Applicants respectfully submit that Scepanovic does not disclose, teach, or even suggest such a method. For instance, Scepanovic does not disclose, teach, or even suggest retrieving multiple pre-computed attributes. Moreover, Applicants have amended claim 54 to recite the limitation that the retrieved attributes include the number of bends in the connection graphs. As discussed above, Scepanovic does not disclose, teach, or even suggest this limitation. Accordingly, Applicants respectfully submit that Scepanovic neither anticipates, nor otherwise invalidates, claim 54. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claim 54.

CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 28, 31-39, 41-52 and 54, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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